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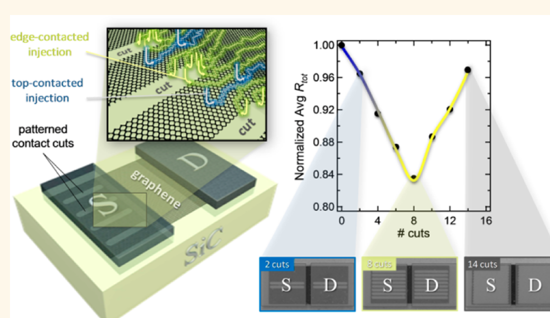
# Reducing Contact Resistance in Graphene Devices through Contact Area Patterning


**Joshua T. Smith,* Aaron D. Franklin, Damon B. Farmer, and Christos D. Dimitrakopoulos**

IBM T.J. Watson Research Center, Yorktown Heights, New York 10598, United States



**ABSTRACT** Performance of graphene electronics is limited by contact resistance associated with the metal—graphene (M—G) interface, where unique transport challenges arise as carriers are injected from a 3D metal into a 2D-graphene sheet. In this work, enhanced carrier injection is experimentally achieved in graphene devices by forming cuts in the graphene within the contact regions. These cuts are oriented normal to the channel and facilitate bonding between the contact metal and carbon atoms at the graphene cut edges, reproducibly maximizing "edge-contacted" injection. Despite the reduction in M—G contact area caused by these cuts, we find that a 32% reduction in contact resistance results in Cu-contacted, two-terminal devices, while a 22% reduction is achieved for top-gated graphene transistors with Pd contacts as compared to conventionally fabricated devices. The crucial role of contact annealing to facilitate this improvement is also elucidated. This simple approach provides a reliable and reproducible means of lowering contact resistance in graphene devices to bolster performance. Importantly, this enhancement requires no additional processing steps.



**KEYWORDS:** graphene transistor · contact · resistance · contact patterning


Graphene has drawn widespread scientific and technological interest that has been fueled by its unique properties,[1−3] such an extremely high intrinsic mobility,[4−6] offering great potential in future high-performance nanoelectronics. To date, graphene has found utility in a broad range of applications, including experimentally demonstrated radio frequency (RF) devices with cutoff frequencies in the hundreds-of-gigahertz range,[7,8] terahertz modulators,[9] interconnects,[10−12] and flexible electronics.[13−15] At this stage, the role of the metal—graphene (M—G) contact is at the forefront of the remaining obstacles hindering further progress in performance.[16−25] Accessing the intrinsic transport properties that graphene has to offer requires that the contact resistance ($R_C$) associated with the M—G interface be very low. State-of-the-art silicon metal-oxide-semiconductor field-effect transistors (MOSFETs) demand a resistance of 80 $\Omega \cdot \mu$m per contact, roughly 10% of the on-resistance of the transistor $V_{DD}/I_{ON}$.[26] Yet, graphene regularly demonstrates $R_C$ values many times this minimum requirement, greatly impeding the potential of graphene-based electronics.

The nature of the $R_C$ problem associated with the M—G interface stems from the unique physical interactions that take place between the contact metal and the atomically thin graphene sheet. Carrier transport in this system can basically be envisioned as two cascading events with resistance contributions associated with each, involving injection from the metal into the underlying graphene followed by transport into the channel region.[18] In the latter event, higher resistance originates from a built-in electrostatic field, which impedes carrier transport into the channel, that forms near the M—G contact just inside the channel as a result of charge transfer doping in the contacted graphene,[22,23] yielding a gate-voltage-dependent asymmetry in the resistance, as this field is modulated by the gate bias.[19] Charge transfer doping takes place due to the work-function difference between the metal and graphene coupled with the small available density of states (DOS) close


*Address correspondence to joshsmit@us.ibm.com.



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to the graphene Fermi level ($E_F$).[21] $E_F$ shifts significantly from the Dirac point, "doping" the graphene, as the two materials come into equilibrium. Other sources of resistance arise from the initial transmission event in which carriers are injected across the M−G interface. Nagashio *et al.* first observed with four-probe measurements that current crowding generally takes place at the edge of the metal/graphene contact, *i.e.*, that contact resistivity $\rho_C$ for graphene is more a function of the graphene width than of area.[16] Though the transfer length $L_T$, or distance over which the potential drops to $1/e$ of the applied $V_{ds}$, is smaller in graphene, it is not negligible and may depend on several factors, including the comparatively smaller DOS available in the graphene under the contact and coupling between the metal and graphene.[18,21] Given the significant increase in the graphene DOS due to charge transfer doping, it may be likely that the weak M−G coupling plays a more dominant role in increasing $R_C$. Indeed, a model that treats the weak electronic interaction of the M−G interfacial region as a thin dielectric layer has been used successfully to describe the electrical behavior of fabricated top/bottom-gated graphene devices;[27] however, the precise nature of the chemical bonding arrangement between various contact metals and graphene remains a subject of theoretical exploration.[23,28−30]

Efforts to enhance transmission from the contact metal into the graphene have led to a breadth of engineering methodologies. One common approach involves exploitation of work-function engineering, using contact metals with a large work-function difference compared to graphene to heavily dope the graphene under the metal, increasing the DOS and thereby reducing $\rho_C$.[16,19,23,31] While the choice of metal greatly impacts $R_C$, it has also become clear that the choice of metal is more complex than work-function engineering alone.[31] Thermal annealing treatments have also proven effective in lowering $R_C$,[31−33] particularly when combined with other techniques, showing dramatic improvements even when the graphene surface in the contact area is contaminated with resist residue.[33] Franklin *et al.* explored a double-contact geometry with contact metals above and below the graphene layer, experimentally demonstrating a decrease in $R_C$ of at least 40% compared to traditional top contacts.[34] This result seems to suggest that weak coupling between the M−G plays the dominant role in increasing $R_C$ as opposed to an insufficient DOS in the graphene. Another method involves low-power $O_2$[31,35] or ultraviolet (UV) ozone[36] to clean the graphene and make the surface hydrophilic as well as to create defects in the graphene contacts prior to metalization, thereby improving the interaction energy between the M−G through chemical bond formation. The drawback of this approach is that the defects are generated in a random fashion, and if process conditions are not properly tuned, this technique can result in significant loss of graphene and/or excessive scattering in the contacted region, leading to degraded $R_C$. Theoretical work proposes that a graphene sheet contacted just at its edges ("end-contacted" graphene) simultaneously results in dramatic improvements in both $R_C$ and mechanical stability of the contact.[29] Experimental efforts, involving the use of a nanoprobe in an ultrahigh-vacuum environment to measure the conductance of graphene flakes at their edge and side locations, have provided some initial confirmation of the "end-contacted" benefit.[37]

In this work, graphene devices are fabricated with cuts lithographically defined in the contact regions, positioned very close and perpendicular to the channel in an effort to reproducibly maximize the perimeter of the graphene edges available for bonding with the contact metal, while leaving the graphene between the cuts undamaged (as shown in Figure 1). Electrical measurements were performed on hundreds of devices to evaluate the efficacy of this approach in reducing $R_C$. Two-terminal devices with Cu contacts and an increased number of contact cuts were fabricated to study the trends in the average total resistance $R_{tot}$ before and after vacuum annealing at 350 °C. Additionally, transfer length method (TLM) structures were parallel processed to account for $R_C$ contributions to the observed trends in $R_{tot}$. Finally, the performance of top-gated graphene FETs (g-FETs) employing standard Pd contacts is compared with and without cuts in the contact regions.

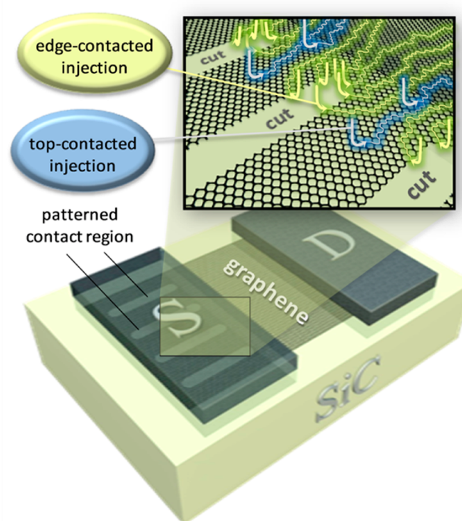


**Figure 1. Schematic representation of a two-terminal graphene device with cuts patterned perpendicular to the channel in the contact region. Enhanced carrier injection occurs along the cut graphene edges (*edge-contacted injection*), where the interaction energy between the metal and carbon atoms is more favorable due to the allowable bonding arrangement at this interface. Normal *top-contacted injection* also takes place.**

## RESULTS AND DISCUSSION

**"Edge-Contacted" Graphene and Role of Contact Annealing.** All devices in this work were created on epitaxial graphene grown on semi-insulating 6H(0001) SiC substrates. As shown in the optical image in Figure 2a, sets of passive graphene resistor devices were fabricated with an increasing number of electron-beam-lithography-defined cuts in the graphene contact regions, where the cuts in each set were varied from zero (uncut) to 14. Note that these cuts are patterned and etched from the contact area in the same fabrication step that is used to isolate each device: an essential step in graphene device fabrication regardless of the graphene source used. In total, the device array consisted of 24 device sets, each containing the full range of variations, which were electrically tested to obtain a good statistical average of $R_{tot}$ for each data point (see Supporting Information). Given the technological relevance to graphene-based interconnects and low associated $R_C$, a 50 nm thick layer of Cu was chosen as the source/drain contact metal.

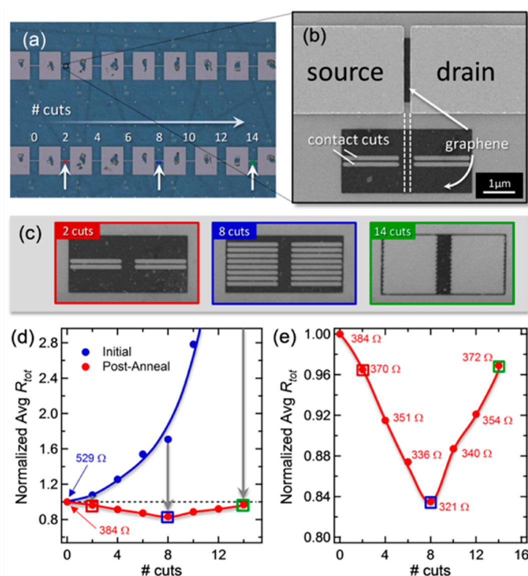


Figure 2. Structure and average total resistance ($R_{tot}$) comparison data for Cu-contacted graphene devices with varied numbers of cuts in the contact areas. (a) Optical image of the graphene device sets, each set containing 0−14 cuts in the source/drain contact regions. All devices have $L_{ch}$ = 300 nm and $W_{ch}$ = 2 $\mu$m. (b) SEM image of a graphene device with two cuts in the contact areas and a duplicate patterned graphene structure fabricated beneath to verify cut dimensions and alignment. (c) SEM images showing typical cut pattern results for 2, 8, and 14 cuts (left to right) in the source and drain regions. Note: 14 cuts resulted in complete removal of graphene from the center of the contact areas. (d) Average $R_{tot}$ before and after a 350 °C vacuum anneal for devices containing 0−14 cuts. Initial and postanneal values are normalized separately to the average $R_{tot}$ of the uncut devices (values indicated); average $R_{tot}$ initially reflects the loss of graphene area (blue), but cut devices improve favorably postanneal (red). (e) Postanneal average $R_{tot}$ (normalized) zoom-in with average values indicated. $R_{tot}$ improves by ∼17% in the best case with eight cuts compared to the benchmark device, where no cuts are present.

A scanning electron microscope (SEM) image of a representative device with two cuts in each contact is shown in Figure 2b. Each device had a designed channel length $L_{ch}$ = 300 nm to ensure that $R_C$ accounted for a large portion of $R_{tot}$ and a channel width $W_{ch}$ = 2 $\mu$m. In all cases, a duplicate graphene structure was patterned directly below the actual device to verify the dimensions of the cuts in the graphene as well as the alignment of the cut edges to the channel region. The cut edges were designed to reside 100 nm from the channel. SEM measurements indicated ∼30 nm alignment accuracy. Figure 2c depicts SEM images of typical duplicate graphene structures having 2, 8, and 14 cuts in each source and drain contact. The patterned contact areas resulted in cut widths $W_{cut} \approx$ 160 nm with graphene nanoribbon widths $W_{GNR} \approx$ 40 nm between each cut. These values applied as long as the cut number was kept to a maximum of eight. For additional cuts, $W_{GNR}$ continued to get smaller until completely vanishing when the cut number reached 14, leaving only jagged graphene edges in close proximity to the channel.

Electrical measurements of the as-fabricated graphene devices initially showed a rapid *increase* in average $R_{tot}$ for an increasing number of cuts; however, this situation reversed dramatically after annealing the devices. Figure 2d displays the initial (preanneal) average $R_{tot}$ values (blue curve) normalized to the average $R_{tot}$ for the uncut devices (529 Ω). Clearly, removal of graphene from the contact areas is reflected by a corresponding increase in $R_{tot}$. A dramatic, almost exponential, increase in $R_{tot}$ takes place for cut numbers greater than eight, possibly due to the narrowing $W_{GNR}$. In fact, the complete removal of graphene between cuts, when the cut number per contact reaches 14, results in an $R_{tot}$ increase by a factor of ∼16.9, or average $R_{tot}$ = 8931 Ω, compared to the uncut devices (see Supporting Information). After subjecting the devices to a 350 °C, high-vacuum anneal, a substantial and universal drop in average $R_{tot}$ was measured. For the uncut devices, the average $R_{tot}$ was reduced to just 384 Ω postanneal, a drop of about 27%. Normalizing the average $R_{tot}$ of the postannealed, cut devices to this new benchmark, Figure 2d shows a remarkable transformation in the trend for devices with patterned contacts (red curve). In all cases, average $R_{tot}$ is less than the uncut devices, including the extreme case of complete graphene removal with 14 cuts where $W_{GNR}$ = 0. Figure 2e shows a zoom-in of the postanneal results along with the average $R_{tot}$ values shown for each variation. A V-shaped trend reveals an unambiguous "sweet spot" for patterned contacts with eight cuts, yielding nearly a 17% reduction in $R_{tot}$.

Significant deductions can be made from the initial and postanneal results. First, we postulate that carrier transmission across the M−G interface is significantly

amplified by bonding with the graphene cut perimeter, an interaction that is enabled by the annealing process. Using first-principles quantum mechanical simulations, Matsuda *et al*. concluded that the incorporation of bifunctional groups (anchors) and p$\pi$ *and* p$\sigma$ orbitals can play substantial roles in improving both cohesion and transmission in "end-contacted" graphene bonded to Cu atoms.[29] While in the present case it is not only the end of the graphene that is contacted as envisioned in this prior study, we argue that our "edge-contacted" graphene around the perimeter of the cuts, which lies beneath the contacts, benefits from the same type of bonding arrangement. Second, the upturn in the V-shape of $R_{tot}$, in the postanneal case, occurs roughly when $W_{GNR}$ begins to narrow below 40 nm. Scattering and energy gap widening play a more substantial role as this happens,[38] which respectively decrease the mobility along the nanoribbons between the cuts and enable a Schottky barrier to form at the M–G interface in these regions, impeding carrier injection. Furthermore, scaling $W_{GNR}$ below the 10–15 nm regime can result in a significant energetic separation between subbands due to quantization effects, which creates another barrier to transport within the nanoribbons and thus limits the potential of $R_C$ reduction. Bearing these caveats in mind, we propose that further improvements in $R_{tot}$ are possible as a direct result of a decreasing $R_C$, by considering an arrangement where $W_{cut}$ is made vanishingly small while $W_{GNR}$ is kept *sufficiently* large, thus striking a balance between the cut density to maximize "edge-contacted" injection and management of quantization effects. Additionally, graphene devices utilizing few-layer graphene can potentially help to mitigate scattering, which considering the larger GNR widths of >25 nm used in this study may be the dominate transport inhibitor. Further experimental and theoretical insights are necessary to quantify the ideal scaling conditions.

**Reducing $R_C$ in Passive Graphene Devices with Cu Contacts.** Two sets of TLM structures were processed on the same sample alongside the previously discussed device sets to quantify the $R_C$ decrease (see Figure 3a), containing either normal (uncut) or patterned (cut) graphene beneath the Cu contacts. Each patterned contact contained 10 cuts, with the cut length extending only 500 nm instead of throughout the entire contact. Duplicate structures were not possible given the layout of the contact leads; however, alignment is assumed to be similar to the aforementioned devices. Eight devices of each type were fabricated and tested to obtain a statistical average. In Figure 3b, the top-view SEM image provides verification of the patterned device dimensions with $L_{ch}$ = 0.15, 0.25, 0.50, 0.75, 1.00, and 1.5 $\mu$m and $W_{ch}$ = 2 $\mu$m.

Initial and postanneal two-terminal electrical measurements were obtained as before, but this time to evaluate $R_C$ using the TLM method.[39] Measurements of average $R_{tot}$ *versus* $L_{ch}$ for normal contacts are plotted in Figure 3c along with linear fits and associated equations. The choice of $W_{ch}$ = 2 $\mu$m permits direct extraction of $R_C$ from the *y*-intercept of the fit equations. In the case of normal contacts, a reduction in $R_C$ from 263 $\Omega\cdot\mu$m to 184 $\Omega\cdot\mu$m, or 30% decrease, occurs when the sample is annealed as done previously. For patterned contacts (Figure 3d), the same anneal facilitates a much more substantial drop of 81% in $R_C$ from 650 $\Omega\cdot\mu$m to 125 $\Omega\cdot\mu$m, which agrees well with the trends discussed above. Perhaps most importantly, comparison of the postanneal results of Figure 3c and d indicates a 32% reduction in $R_C$ for the patterned devices compared to those with normal contacts, representing a significant performance enhancement in graphene-based electronics. Note that the advantage may be much more pronounced when patterning is applied to structures, such as interconnects, where more than one graphene sheet is present. The interlayer resistance $R_{int}$ between graphene sheets in few-layer and multilayer g-FETs has been estimated to be $R_{int} \approx 105\ \Omega$,[40] whereas contact patterning would enable a bypass to this resistance contribution, providing "edge-contacted" access to each individual graphene sheet within the stack.

The sheet resistance of the graphene channel $R_S$ can be determined using the TLM approach and is

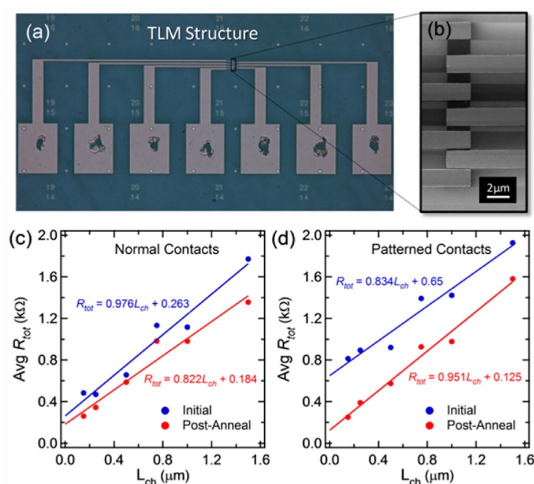


**Figure 3. TLM structure for Cu-contacted graphene devices with accompanying characterization results for normal and patterned contacts both before and after annealing. (a) Optical and (b) SEM images of graphene TLM structures with Cu contacts. $L_{ch}$ variations are 0.15, 0.25, 0.50, 0.75, 1.0, and 1.5 $\mu$m. Structures were fabricated with devices that contained no cuts, *i.e.*, "normal contacts", and 10 cuts, *i.e.* "patterned contacts" in the contact areas (cuts not shown). (c) Average $R_{tot}$ for TLM devices with *normal contacts* before and after a 350 °C vacuum anneal. Contact resistance drops 30% from 263 $\Omega\cdot\mu$m to 184 $\Omega\cdot\mu$m with an anneal. (d) Average $R_{tot}$ for TLM devices with *patterned contacts* before and after annealing. $R_C$ drops 81% from 650 $\Omega\cdot\mu$m to just 125 $\Omega\cdot\mu$m postanneal. Postanneal results indicate a 32% reduction in $R_C$ compared to postannealed normal contacts (benchmark devices).**

given by the equation $R_{tot} = (R_S/W_{ch})L_{ch} + 2R_C/W_{ch}$, meaning $R_S = 1644$ and 1902 Ω/□ for the postannealed normal and patterned devices, respectively. These values correspond to a relatively low channel doping with a rough estimate of carrier density $N_{2D} \approx 10^{12}$ cm$^{-3}$ and mobility $\mu \approx 3300-3800$ cm$^2$/V·s (see Supporting Information), which is in agreement with Hall bar measurements performed on graphene grown using the same epitaxial growth system and process conditions.[41] Unfortunately, since the sheet resistance in the channel and beneath the contact are significantly different for graphene devices, the TLM method cannot be used to accurately derive $L_T$.[18] The situation is further complicated by the presence of the cuts and disparate transmission probabilities of edge- *versus* top-contacted injection. Nevertheless, by altering the 100 nm design distance of the cut edges from the channel and optimizing the cut width and density as mentioned above, it may be possible to even further lower $R_C$ using the patterned contact approach.

**$R_C$ Reduction in Graphene Transistors with Pd Contacts.** As shown in Figure 4a, top-gated g-FETs with patterned graphene contacts and a Pd contact metal were also fabricated in a TLM configuration in order to extract $R_C$. Once again, devices with normal contacts were also processed on the same sample and tested as a benchmark. Pd was utilized to verify the benefit of contact area patterning using a different and more commonly used contact metal. The gate stack consisted of an $AlO_xN_y$ seed layer and 10 nm thick $HfO_2$ gate dielectric followed by Ti/Pd/Au (0.5 nm/20 nm/20 nm) gate metal layers with a 100 nm gate overlap. Cuts were patterned using the same process conditions and dimensions as in the previous sample also having $W_{ch} = 2$ $\mu$m. Devices with patterned contacts for this sample all contained the optimized eight cuts.

Collective transfer curves for transistors with $L_{ch} = 1$ $\mu$m swept over a gate voltage $V_{gs}$ range of $-3$ to 4 V at $V_{ds} = -10$ mV are given in Figure 4b and c for normal and patterned contacts, respectively. The n-type behavior with only the electron branch accessible within the gate voltage sweep range is typical of epitaxial graphene grown on SiC,[42] where dangling bonds associated with the buffer layer may act as positive charge traps.[43] The small $I_{ON}/I_{OFF}$ ratio ranging from 1.4 to 1.8 for all devices tested may indicate additional doping or scattering from the $AlO_xN_y$ seed layer. Perhaps the most obvious contrast in Figure 4b and c is the considerable improvement in device-to-device consistency for transistors featuring patterned contacts. This attribute is found to apply universally for all devices tested. Figure 4d illustrates this trend well, showing the average $I_{ON}$ with min−max range for normal and patterned devices with $L_{ch} = 1, 2, 3, 4, 5,$ and 6 $\mu$m. Since the Dirac point is inaccessible in these devices, $I_{ON}$ values were extracted from each transfer curve relative to the maximum transconductance

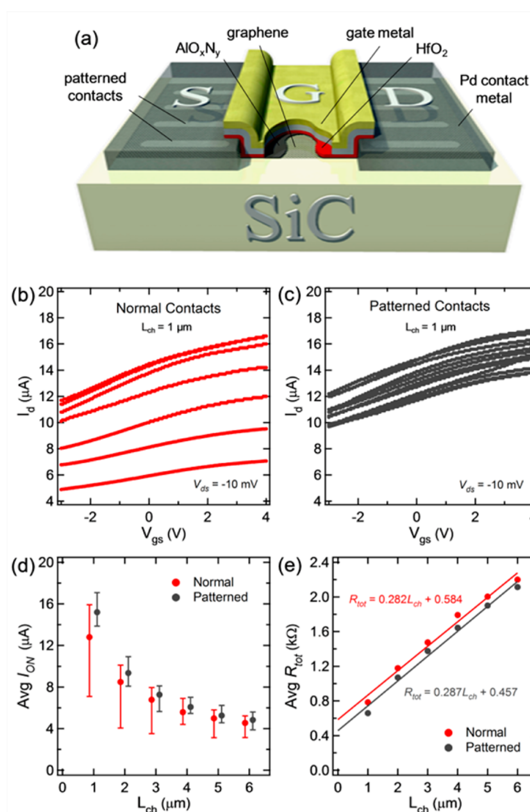


**Figure 4. Structure and characteristic trends of top-gated graphene field-effect transistors (g-FETs) with normal and patterned Pd contacts. (a) Schematic of a top-gated g-FET with patterned contacts, showing the $AlO_xN_y/HfO_2$/Ti/Pd/Au (1 nm/10 nm/0.5 nm/20 nm/20 nm) gate stack. Collective transfer curves for n-type g-FETs having (b) normal and (c) patterned contacts with $L_{ch} = 1$ $\mu$m, with the patterned contact transistors showing a significant improvement in device-to-device consistency as well as greater overall current drive. (d) Average $I_{ON}$ with min−max distribution for normal and patterned devices having $L_{ch} = 1, 2, 3, 4, 5,$ and 6 $\mu$m. $I_{ON}$ values were extracted from transfer characteristics at $V_{gs} - V_{gm_max} = 4$ V. Patterned contact g-FETs show a tighter distribution and improved average $I_{ON}$. (e) Average $R_{tot}$ for g-FETs with normal and patterned contacts and TLM method extraction of $R_C$. Patterned contact devices demonstrate a ∼22% reduction in $R_C$ compared to normal contacts.**

voltage ($V_{gm_max}$), specifically $I_{ON}$ ($V_{gs} - V_{gm_max} = 4$ V) (see Supporting Information). Better consistency in g-FETs with patterned contacts may be an indication of the improved mechanical stability expected for "end-contacted" graphene.[29] In addition, Figure 4d shows that the patterned approach offers an advantage in terms of enhanced average $I_{ON}$ as a result of the improved transmission. This translates to a boost in average $g_{m_max}$ ranging from 3.5% to 12% for the chosen channel lengths. We emphasize that the minimum channel length for the fabricated g-FETs is 1 $\mu$m and note that greater improvements in both $I_{ON}$ and $g_m$ are expected as the channel length is scaled, where $R_C$ becomes increasingly dominant.

A transfer length plot is shown in Figure 4e for normal and patterned contacts that reconfirms the

significance of the contact patterning approach for decreasing $R_C$, where $R_{tot} = I_{ON}/V_{ds}$. $R_C$ for these Pd contacts decreases from 584 $\Omega\cdot\mu$m to 457 $\Omega\cdot\mu$m when patterning is applied to the graphene contact areas, representing a ~22% reduction in $R_C$. It is theoretically projected that the benefits of Pd contacts are not as impactful as Cu,[29] a conclusion that is supported in this study; however, the margin of improvement is still substantial. The $R_S$ distribution is much tighter in these top-gated devices, ranging from 564 to 574 Ω/□, indicating an expected high level of doping from the presence of the seed layer with an approximate minimum carrier density $N_{2D} \approx 9 \times 10^{12}$ cm$^{-3}$ and maximum mobility $\mu \approx 1220$ cm$^2$/V·s.

## CONCLUSIONS

By applying contact patterning in the form of cuts in the contact regions of a graphene device, a new "edge-contacted" method to reproducibly increase the performance of graphene electronics was experimentally verified for Pd and Cu contact metals, reducing average $R_C$ by as much as 22−32%. Further, greater device-to-device consistency was observed in graphene transistors using this technique, an important feature for implementation of any potential graphene-based technology. The process steps are advantageously identical to that of normal graphene devices and readily compatible with any graphene device regardless of the source of graphene. This approach may be combined with other techniques, such as metal contact engineering, annealing, and gentle UV ozone cleaning, and therefore lays a foundation for further progress in graphene device performance as well as fundamental studies related to the transport mechanisms associated with this unique contact geometry.

## METHODS

**Epitaxial Graphene Growth.** Epitaxial graphene was grown on semi-insulating 6H(0001) SiC wafer surfaces within a cylindrical, induction-heated graphite susceptor installed in a ultrahigh-vacuum chamber. We used a multistep process comprising two surface preparation steps, annealing at 810 °C for 10 min and 1140 °C for 7 min (both under the flow of 20% disilane in He), and a graphenization step, heating at 1550 °C for 10 min under Ar flow at a chamber pressure of 3.5 mTorr.[42,44]

**Graphene Device Fabrication.** Following graphene growth, electron-beam lithography (EBL) was used to pattern the graphene into hundreds of 4.3 $\mu$m × 2 $\mu$m (length × width) rectangles with and without cuts in the source/drain contact regions, implementing poly(methyl methacrylate) A4 (PMMA) (MicroChem) as a mask for subsequent oxygen plasma etching to define the graphene. After graphene etching, the PMMA layer was removed with 80 °C acetone and an isopropyl alcohol rinse. A second EBL step was used to create source/drain contacts that were well-aligned to the contact cuts. For two-terminal devices, contacts were defined by a 50 nm thick, electron-beam evaporated Cu layer and lift-off in 80 °C acetone to complete fabrication. In the case of g-FETs, contacts were achieved in a similar manner but with a two-step EBL process to ensure pure Pd contacts, involving a Ti/Pd/Au (0.5 nm/15 nm/20 nm) stack to define the probe pads and larger leads and a second e-beam evaporation of 50 nm thick Pd for direct graphene contact. The gate stack was deposited, first by atomic layer deposition (ALD) of a ~1 nm $AlO_xN_y$ seed layer and 10 nm $HfO_2$ gate dielectric and second by a fourth EBL step to define a Ti/Pd/Au (0.5 nm/20 nm/20 nm) gate metal stack with a 100 nm overlap. Using a Cascade Summit semiautomated probe station, the hundreds of devices were then tested in air. For two-terminal devices, a 350 °C, 15 h high-vacuum anneal at ~$5 \times 10^8$ Torr was applied, after which the devices were again tested in the same manner. Contact annealing for the g-FETs was carried out as part of the ALD process.

**ALD Formation of the Top-Gate Dielectric Stack.** The gate dielectric is deposited by ALD. The graphene surface is first functionalized to allow for uniform ALD by applying a ~1 nm thick seed layer of $AlO_xN_y$ (10 cycles of $NO_2$, trimethylaluminum, and water vapor sequentially deposited) at room temperature.[45] After deposition, the seed layer is annealed at 300 °C for eight hours under vacuum (300 mTorr) in flowing Ar. This is followed by 10 nm $HfO_2$ ALD (tetrakis(dimethylamido)hafnium and water vapor) at 125 °C.

*Conflict of Interest:* The authors declare no competing financial interest.

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*Supporting Information Available:* Additional experiment details. This material is available free of charge *via* the Internet at http://pubs.acs.org.

## REFERENCES AND NOTES

1. Lee, C.; Wei, X.; Kysar, J. W.; Hone, J. Measurement of the Elastic Properties and Intrinsic Strength of Monolayer Graphene. *Science* **2008**, *321*, 385–388.
2. Meric, I.; Han, M. Y.; Young, A. F.; Ozyilmaz, B.; Kim, P.; Shepard, K. L. Current Saturation in Zero-Bandgap, Top-Gated Graphene Field-Effect Transistors. *Nat. Nanotechnol.* **2008**, *3*, 654–659.
3. Murali, R.; Yang, Y.; Brenner, K.; Beck, T.; Meindl, J. D. Breakdown Current Density of Graphene Nanoribbons. *Appl. Phys. Lett.* **2009**, *94*, 243114-1–3.
4. Novoselov, K. S.; Geim, A. K.; Morozov, S. V; Jiang, D.; Zhang, Y.; Dubonos, S. V; Grigorieva, I. V; Firsov, A. A. Electric Field Effect in Atomically Thin Carbon Films. *Science* **2004**, *306*, 666–669.
5. Bolotin, K. I.; Sikes, K. J.; Jiang, Z.; Klima, M.; Fudenberg, G.; Hone, J.; Kim, P.; Stormer, H. L. Ultrahigh Electron Mobility in Suspended Graphene. *Solid State Commun.* **2008**, *146*, 351–355.
6. Du, X.; Skachko, I.; Barker, A.; Andrei, E. Y. Approaching Ballistic Transport in Suspended Graphene. *Nat. Nanotechnol.* **2008**, *3*, 491–495.
7. Lin, Y.-M.; Dimitrakopoulos, C.; Jenkins, K. A.; Farmer, D. B.; Chiu, H.-Y.; Grill, A.; Avouris, P. 100-GHz Transistors from Wafer-Scale Epitaxial Graphene. *Science* **2010**, *327*, 662.
8. Liao, L.; Lin, Y.-C.; Bao, M.; Cheng, R.; Bai, J.; Liu, Y.; Qu, Y.; Wang, K. L.; Huang, Y.; Duan, X. High-Speed Graphene Transistors with a Self-Aligned Nanowire Gate. *Nature* **2010**, *467*, 305–308.
9. Sensale-Rodriguez, B.; Yan, R.; Kelly, M. M.; Fang, T.; Tahy, K.; Hwang, W. S.; Jena, D.; Liu, L.; Xing, H. G. Broadband Graphene Terahertz Modulators Enabled by Intraband Transitions. *Nat. Commun.* **2012**, *3*, 780.
10. Chen, X.; Akinwande, D.; Lee, K.; Close, G. F.; Yasuda, S.; Paul, B. C.; Fujita, S.; Kong, J.; Wong, H.-S. P. Fully Integrated Graphene and Carbon Nanotube Interconnects for

Gigahertz High-Speed CMOS Electronics. *IEEE Trans. Electron Devices* **2010**, *57*, 3137–3143.
11. Murali, R.; Brenner, K.; Yang, Y. Resistivity of Graphene Nanoribbon Interconnects. *IEEE Electron Device Lett.* **2009**, *30*, 611–613.
12. Li, H.; Xu, C.; Srivastava, N.; Banerjee, K. Carbon Nanomaterials for Next-Generation Interconnects and Passives: Physics, Status, and Prospects. *IEEE Trans. Electron Devices* **2009**, *56*, 1799–1821.
13. Kim, B. J.; Jang, H.; Lee, S.-K.; Hong, B. H.; Ahn, J.-H.; Cho, J. H. High-Performance Flexible Graphene Field Effect Transistors with Ion Gel Gate Dielectrics. *Nano Lett.* **2010**, *10*, 3464–3466.
14. Nayfeh, O. M. Graphene Transistors on Mechanically Flexible Polyimide Incorporating Atomic-Layer-Deposited Gate Dielectric. *IEEE Electron Device Lett.* **2011**, *32*, 1349–1351.
15. Gomez De Arco, L.; Zhang, Y.; Schlenker, C. W.; Ryu, K.; Thompson, M. E.; Zhou, C. Continuous, Highly Flexible, and Transparent Graphene Films by Chemical Vapor Deposition for Organic Photovoltaics. *ACS Nano* **2010**, *4*, 2865–2873.
16. Nagashio, K.; Nishimura, T.; Kita, K.; Toriumi, A. Metal/Graphene Contact as a Performance Killer of Ultra-High Mobility Graphene - Analysis of Intrinsic Mobility and Contact Resistance. *IEDM Tech. Dig.* **2009**, 565–568.
17. Cayssol, J.; Huard, B.; Goldhaber-Gordon, D. Contact Resistance and Shot Noise in Graphene Transistors. *Phys. Rev. B* **2009**, *79*, 075428-1−6.
18. Xia, F.; Perebeinos, V.; Lin, Y.-M.; Wu, Y.; Avouris, P. The Origins and Limits of Metal-Graphene Junction Resistance. *Nat. Nanotechnol.* **2011**, *6*, 179–184.
19. Huard, B.; Stander, N.; Sulpizio, J.; Goldhaber-Gordon, D. Evidence of the Role of Contacts on the Observed Electron-Hole Asymmetry in Graphene. *Phys. Rev. B* **2008**, *78*, 121402−1−4.
20. Franklin, A. D.; Han, S.-J.; Bol, A. A.; Haensch, W. Effects of Nanoscale Contacts to Graphene. *IEEE Electron Device Lett.* **2011**, *32*, 1035–1037.
21. Nagashio, K.; Toriumi, A. Density-of-States Limited Contact Resistance in Graphene Field-Effect Transistors. *Jpn. J. Appl. Phys.* **2011**, *50*, 070108-1−6.
22. Russo, S.; Craciun, M. F.; Yamamoto, M.; Morpurgo, A. F.; Tarucha, S. Contact Resistance in Graphene-Based Devices. *Phys. E (Amsterdam, Neth.)* **2010**, *42*, 677–679.
23. Giovannetti, G.; Khomyakov, P. A.; Brocks, G.; Karpan, V. M.; Van den Brink, J.; Kelly, P. J. Doping Graphene with Metal Contacts. *Phys. Rev. Lett.* **2008**, *101*, 026803-1−4.
24. Lee, E. J. H.; Balasubramanian, K.; Weitz, R. T.; Burghard, M.; Kern, K. Contact and Edge Effects in Graphene Devices. *Nat. Nanotechnol.* **2008**, *3*, 486–490.
25. Venugopal, A.; Colombo, L.; Vogel, E. M. Contact Resistance in Few and Multilayer Graphene Devices. *Appl. Phys. Lett.* **2010**, *96*, 013512-1−3.
26. The National Technology Roadmap for Semiconductors, Semiconductor Industry Association , **2010**.
27. Berdebes, D.; Member, S.; Low, T.; Sui, Y.; Appenzeller, J.; Lundstrom, M. S. Substrate Gating of Contact Resistance in Graphene Transistors. *IEEE Trans. Electron Devices* **2011**, *58*, 3925–3932.
28. Vanin, M.; Mortensen, J. J.; Kelkkanen, A. K.; Garcia-Lastra, J. M.; Thygesen, K. S.; Jacobsen, K. W. Graphene on Metals: A van der Waals Density Functional Study. *Phys. Rev. B* **2010**, *81*, 081408−1−4.
29. Matsuda, Y.; Deng, W.-Q.; Goddard, W., III. Contact Resistance for "End-Contacted" Metal-Graphene and Metal-Nanotube Interfaces from Quantum Mechanics. *J. Phys. Chem. C* **2010**, *114*, 17845–17850.
30. Gong, C.; Lee, G.; Shan, B.; Vogel, E. M.; Wallace, R. M.; Cho, K. First-Principles Study of Metal−Graphene Interfaces. *J. Appl. Phys.* **2010**, *108*, 123711-1−8.
31. Robinson, J. A.; LaBella, M.; Zhu, M.; Hollander, M.; Kasarda, R.; Hughes, Z.; Trumbull, K.; Cavalero, R.; Snyder, D. Contacting Graphene. *Appl. Phys. Lett.* **2011**, *98*, 053103–1−3.
32. Balci, O.; Kocabas, C. Rapid Thermal Annealing of Graphene-Metal Contact. *Appl. Phys. Lett.* **2012**, *101*, 243105–1−5.
33. Malec, C. E.; Elkus, B.; Davidović, D. Vacuum-Annealed Cu Contacts for Graphene Electronics. *Solid State Commun.* **2011**, *151*, 1791–1793.
34. Franklin, A. D.; Han, S.-J.; Bol, A. A.; Perebeinos, V. Double Contacts for Improved Performance of Graphene Transistors. *IEEE Electron Device Lett.* **2012**, *33*, 17–19.
35. Choi, M. S.; Lee, S. H.; Yoo, W. J. Plasma Treatments to Improve Metal Contacts in Graphene Field Effect Transistor. *J. Appl. Phys.* **2011**, *110*, 073305-1–6.
36. Wei Chen, C.; Ren, F.; Chi, G.-C.; Hung, S.-C.; Huang, Y. P.; Kim, J.; Kravchenko, I. I.; Pearton, S. J. UV Ozone Treatment for Improving Contact Resistance on Graphene. *J. Vac. Sci. Technol. B* **2012**, *30*, 060604-1–3.
37. Wu, Y.; Wang, Y.; Wang, J.; Zhou, M.; Zhang, A.; Zhang, C.; Yang, Y.; Hua, Y.; Xu, B. Electrical Transport across Metal/Two-Dimensional Carbon Junctions: Edge versus Side Contacts. *AIP Adv.* **2012**, *2*, 012132-1–12.
38. Han, M.; Özyilmaz, B.; Zhang, Y.; Kim, P. Energy Band-Gap Engineering of Graphene Nanoribbons. *Phys. Rev. Lett.* **2007**, *98*, 206805-1–4.
39. Berger, H. H. Models for Contacts to Planar Devices. *Solid-State Electron.* **1972**, *15*, 145–158.
40. Sui, Y.; Appenzeller, J. Screening and Interlayer Coupling in Multilayer Graphene Field-Effect Transistors. *Nano Lett.* **2009**, *9*, 2973–2977.
41. Dimitrakopoulos, C.; Liu, G.; McArdle, T. J.; Grill, A.; Smith, J. T.; Farmer, D. B.; Avouris, P.; Pfeiffer, D. Wafer-Scale Epitaxial Graphene and Graphene Nanoribbon Arrays on SiC. Extended abstract book, Graphene Conference: From Research to Applications, 15-16 October 2012, National Physical Laboratory Teddington, Middlesex, UK. http://www.npl.co.uk/science-technology/quantum-detection/news-events/graphene-conference-2012/graphene-conference-2012-agenda/.
42. Dimitrakopoulos, C.; Lin, Y.-M.; Grill, A.; Farmer, D. B.; Freitag, M.; Sun, Y.; Han, S.-J.; Chen, Z.; Jenkins, K. A.; Zhu, Y.; *et al.* Wafer-Scale Epitaxial Graphene Growth on the Si-Face of Hexagonal SiC (0001) for High Frequency Transistors. *J. Vac. Sci. Technol. B* **2010**, *28*, 985–992.
43. Farmer, D.; Perebeinos, V.; Lin, Y.-M.; Dimitrakopoulos, C.; Avouris, P. Charge Trapping and Scattering in Epitaxial Graphene. *Phys. Rev. B* **2011**, *84*, 205417-1–5.
44. Dimitrakopoulos, C.; Grill, A.; McArdle, T. J.; Liu, Z.; Wisnieff, R.; Antoniadis, D. A. Effect of Sic Wafer Miscut Angle on the Morphology and Hall Mobility of Epitaxially Grown Graphene. *Appl. Phys. Lett.* **2011**, *98*, 222105-1–3.
45. Lin, Y.-M.; Jenkins, K. A.; Valdes-Garcia, A.; Small, J. P.; Farmer, D. B.; Avouris, P. Operation of Graphene Transistors at Gigahertz Frequencies. *Nano Lett.* **2009**, *9*, 422–426.